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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/359,056	07/21/1999	BARMAK MANSOORIAN	08305/038001	2286

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	12

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/359,056	MANSOORIAN, BARMAK	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 4, 5, 7, 8, 10, 11 & 14 are objected to:

Regarding claim 4, claim 4 recites the limitation "the current bias" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 5, 8 & 11, the claims are objected as dependent claims of claim 4.

Regarding claim 7, claim 7 recites the limitation "the current bias" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 10, claim 10 recites the limitation "the current bias" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 14, claim 14 recites the limitation "said an image acquisition portion" in lines 1-2 of the claim, which should be changed to – said image acquisition portion – .

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Sim et al (US 6,075,384).

Regarding claim 1, Pain discloses an image sensor, comprising:

an image acquisition portion (100, 112) as shown in figs. 1A-1C, col. 3, lines 52-63;

an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current mode output (see fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output because such impedance must exist in all transmission lines of electrical signals, especially the digital output 110 of ADC array in current mode driving, meaning that the output impedance is a must.

Pain's disclosure of digital output 110, in figs. 1A-1C, suggests another separate portion, such as another chip, in order for the digital image data to be properly transferred out from the image processing portion (ADC array 118) to the separate portion as "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs...and said image receiving portion receiving current mode output" in order to form a complete imaging system of CMOS compatible applications (see col. 2, lines 5-7 for a consistent CMOS compatible).

Therefore, it would have been obvious to one of ordinary skill in the art to recognize another separate portion, such as another chip, at the digital output from the image processing portion (ADC array 118) as an image receiving portion having CMOS and input characteristics

which are compatible with the digital output of the image processing portion in a complete imaging system.

Pain does not disclose an impedance matching device, matching said output impedance of said image processing portion to said input impedance of said image receiving portion.

In other disclosure, Sim teaches an impedance matching portion (i.e., current mode buffer driver) for matching output impedance of one chip (i.e., digital output of chip 100A) to other chip (i.e., digital input of chip 100B) in current driving mode (see fig. 2; col. 1, lines 10-15; col. 4, lines 41-46 & col. 5, lines 23-28).

It would eliminate reflected waves which may be generated at radio frequencies; therefore providing capable of transmitting data between chips at high speed while reducing power dissipation and increasing signal integrity as suggested by Sim in col. 5, lines 23-28 & col. 2, lines 27-30.

Therefore, it would have been obvious to one of ordinary skill in the art to provide the impedance matching device taught by Sim as a current mode buffer driver at the output of Pain's ADC array to drive digital output to a receiving portion so that it would eliminate reflected waves which may be generated at radio frequencies therefore providing capable of transmitting data between chips at high speed while reducing power dissipation and increasing signal integrity.

Regarding claim 2, the image processing portion includes a portion (impedance matching portion of current mode buffer driver) with a CMOS output (see Sim in fig. 2; col. 4, lines 35-45 for CMOS output M1 & M2).

Regarding claim 3, combined circuits of Sim and Pain provide the impedance matching circuit comprising a circuit on said image processing circuit, meaning that the impedance matching circuit of current mode buffer driver of Sim, as shown in fig. 2, has already been included as a current mode buffer driver at the output of ADC array for driving digital output 110 as shown by Pain in fig. 1C.

Regarding claim 4, the combined circuits of Sim and Pain provide the output of said image processing circuit including a current biased transistor (M1), wherein a magnitude of the current bias (Io1) sets the output impedance (see Sim in fig. 2; col. 5, lines 23-28 & Table 2). It is noted that the output impedance depends upon the reciprocal of the transconductance (gm), in which the transconductance (gm) is not only directly controlled by the size of transistor (M1) but is also controlled by the current bias (Io1). This is clearly shown by Sim in fig. 2 and Table 2 with the current bias Io1 of M1 at OUT1 and the current bias Io2 of M1 at OUT2 being maintained equal at all times for matching output/input impedance.

Regarding claim 5, the output impedance is matched with input impedance of the image receiving circuit (see Sim in fig. 2; col. 5, lines 23-27; Table 2 and the analysis in claim 4, wherein both sides of transmitting and receiving output impedances have the same impedance characteristics).

Regarding claim 6, the impedance matching circuit comprises a circuit on the image receiving circuit (see Sim in fig. 2 for impedance matching circuit at chip 100B).

Regarding claim 7, see claim 4 for the same analysis for output/input impedance matching utilizing current bias Io2 of M1 on chip 100B side.

Regarding claim 8, see claim 5 for the same analysis for output/input matching impedance.

Regarding claim 9, the impedance matching circuit comprises a first circuit on said image processing circuit and a second circuit on said receiving circuit (see Sim in fig. 2 for matching impedance circuits on both sides of chips 100A & 100B).

Regarding claim 10, Sim discloses that both of said first and second circuits include biased elements (M1 on 100A and M1 on 100B), and wherein a magnitude of the current bias sets the output impedance (see fig. 2 for Io1, Io2 and 1/gm, Zo and the analysis in claims 4 & 7).

Regarding claim 11, see claims 5 and 8 for the same limitation and analysis.

Regarding claim 12, Sim discloses that the image receiving circuit (on chip 100B side) includes a current mirror part (M1 & M2), that mirrors the input current (see fig. 2).

Regarding claim 13, Pain discloses the image acquisition circuit being an active pixel sensor (APS 300) with a photosensor (photogate 310), an in-pixel buffer (floating diffusion 330), and in-pixel select transistor (vertical select 370) (see fig. 3A; col. 6, lines 25-49).

Regarding claim 14, Pain also discloses that the image acquisition portion and the image processing portion operates at substantially zero voltage since the CMOS APS pixel and ADC array are driven in current mode, which means voltage required is very small, i.e. 0.5V for driving threshold of M1 (see col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16).

Regarding claim 15, the claimed limitations are analyzed with respect to claim 1. In addition, Sim further discloses adjusting bias current (Io1) through at least one biased device (M1) in a way that renders the impedance relatively independent of input current (I1, I2) (see fig. 2; col. 8, lines 3-5, 8-9, in which the impedance is adjusted as analyzed with respect to claims 4 & 7).

Regarding claim 16, Sim discloses that the image acquisition portion and the image processing portion each operate in current mode (see col. 1, lines 10-15).

Regarding claim 17, the claimed limitation is analyzed with respect to claim 14.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

NT.
April 17, 2003

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600